

WHAT IS CLAIMED IS:

1 1. In an integrated circuit having a substrate and a plurality of stacked
2 metal layers thereover, said metal layers delineated as interconnections for said integrated
3 circuit, a capacitor structure between adjacent stacked metal layers comprising
4 a portion of a first selected one of said stacked metal layers and a portion of a
5 second selected one of said stacked metal layers, said second selected stacked metal layer
6 portion above and adjacent said first selected stacked metal layer portion;
7 a first capacitor dielectric layer over said first selected stacked metal layer
8 portion;
9 a first capacitor metal plate layer over said first capacitor dielectric layer;
10 a second capacitor dielectric layer under said second selected stacked metal
11 layer portion;
12 a second capacitor metal plate layer under said second capacitor dielectric
13 layer and over and removed from said first capacitor metal plate layer; and
14 a metal capacitor via layer between and connecting said first capacitor metal
15 plate layer and said second capacitor metal plate layer, said metal capacitor via layer forming
16 a first terminal of said capacitor structure; and
17 a first via connecting said first selected stacked metal layer portion and said
18 second selected stacked metal layer portion to form a second terminal of said capacitor
19 structure.

1 2. The integrated circuit of claim 1 wherein at least one of said first or
2 second stacked metal layers comprises a plurality of stacked, contiguous metal layers of
3 differing composition.

1 3. The integrated circuit of claim 1 wherein said first capacitor dielectric
2 layer and said first capacitor metal plate layer are laterally co-extensive.

1 4. The integrated circuit of claim 1 wherein said second capacitor
2 dielectric layer and said second capacitor metal plate layer are laterally co-extensive.

1 5. The integrated circuit of claim 4 wherein said first capacitor dielectric
2 layer, said first capacitor metal plate layer, said second capacitor dielectric layer and said
3 second capacitor metal plate layer are laterally co-extensive.

1 6. The integrated circuit of claim 1 wherein said metal capacitor via layer
2 is connected to another portion of said second selected stacked metal layer to form a
3 connection to said second capacitor structure terminal.

1 7. The integrated circuit of claim 1 further comprising a metal layer
2 laterally co-extensive with said first capacitor dielectric layer and said first capacitor metal
3 plate layer, and arranged between said first capacitor dielectric layer and said first selected
4 stacked metal layer portion so that said metal layer forms a plate for said first capacitor.

1 8. The integrated circuit of claim 1 further comprising a metal layer
2 laterally co-extensive with said second capacitor dielectric layer and said second capacitor
3 metal plate layer, and arranged between said second capacitor dielectric layer and said second
4 selected stacked metal layer portion so that said metal layer forms a plate for said second
5 capacitor.

1 9. A method of manufacturing a capacitor structure between first and
2 second metallic interconnections of an integrated circuit, said first and second metallic
3 interconnections separated by an insulating intermetallic oxide layer, said method comprising
4 disposing a first metal-dielectric-metal layer capacitor over and with a portion
5 of said first metallic interconnection portion;

6 disposing a second metal-dielectric-metal layer capacitor under and with a
7 portion of said second metallic interconnection; and

8 disposing a first metal via through said insulating intermetallic oxide layer to
9 connect said first metal-dielectric-metal layer capacitor and said second metal-dielectric-
10 metal layer capacitor, said first metal via layer forming a first terminal of said capacitor
11 structure; and

12 disposing a second metal via through said insulating intermetallic oxide layer
13 to connect said first metallic interconnection and said second metallic interconnection portion
14 to form a second terminal of said capacitor structure.

1 10. The method of claim 9 wherein in said first metal disposing step, said
2 first metal via further connects to at least one of said first and second metallic
3 interconnections.

1 11. The method of claim 9 wherein in said first metal-dielectric-metal
2 layer capacitor disposing step, said first metal-dielectric-metal layer capacitor comprises said
3 first metallic interconnection portion, a capacitor dielectric layer on said first metallic
4 interconnection portion, and an upper metal layer on said capacitor dielectric layer.

1 12. The method of claim 9 wherein in said first metal-dielectric-metal
2 layer capacitor disposing step, said first metal-dielectric-metal layer capacitor comprises a
3 lower metal layer on said first metallic interconnection portion, a capacitor dielectric layer on
4 said lower metal layer, and an upper metal layer on said capacitor dielectric layer.

1 13. The method of claim 9 wherein in said second metal-dielectric-metal
2 layer capacitor disposing step, said second metal-dielectric-metal layer capacitor comprises a
3 lower metal layer, a capacitor dielectric layer on said lower metal layer, and said second
4 metallic interconnection portion on said capacitor dielectric layer.

1 14. The method of claim 9 wherein in said second metal-dielectric-metal
2 layer capacitor disposing step, said second metal-dielectric-metal layer capacitor comprises a
3 lower metal layer, a capacitor dielectric layer on said lower metal layer, and an upper metal
4 layer on said capacitor dielectric layer, said second metallic interconnection portion on said
upper metal layer.